REMARKS

Present Status of the Application

Claims 1-2 and 8-10 remain pending in the present application of which claims 1, 2, and 8-9 have been amended and claims 21-22 have been added for more explicitly describing the claimed invention. Amendments to claims 1 and 8 are well supported at paragraphs [0020] and [0021]. It is believed that no new matter adds by way of the amendments to claims or otherwise to the application. For at least the following reasons, Applicants respectfully submit claims 1-2, 8-10 and 21-22 are in proper condition for allowance and reconsideration of this application is respectfully requested.

Discussion of the claim rejection under 35 USC 112

The Office Action rejected claim 9 under 35 U.S.C. 112, second paragraph, because the phrase "the solid indium chloride" lacks antecedent basis.

In response thereto, Applicants would like to thank the Examiner for pointing out the informality and accordingly amended claim 9. Reconsideration is respectfully requested.

Discussion of the claim rejection under 35 USC 102

The Office Action rejected claim 1 under 35 USC 102(e) as being anticipated by Matsuo et al. (US-2004/0000695 A1, hereinafter Matsuo).

Applicants respectfully disagree and would like to point out that rejection under 35 U.S.C. 102 requires that each and every element of the claim(s) must be disclosed

exactly by a single prior art reference. Claim 1, as amended, is allowable for at least the reason that Matsuo fails to teach or disclose a method of manufacturing an N-channel metal-oxide-semiconductor (NMOS) transistor with an P-type gate comprising at least a step of forming an indium doped polysilicon layer over the gate dielectric layer by using a chemical vapor deposition process using a gas comprising indium chloride ($InCl_3$). The advantage of the above process step is that at least the ion implantation for implanting the indium ions and the annealing operation for diffusing indium ions into the polysilicon layer after ion implantation step can be effectively avoided. Furthermore, by using indium chloride ($InCl_3$) gas to form an indium doped polysilicon layer over the gate dielectric layer, the bondage between the indium, the polysilicon layer and gate the silicon oxide layer can be greatly improved.

According to the present inventors, the conventional technique of implanting the indium ions into the polysilicon layer and then annealing for diffusing the indium ions into the polysilicon layer cause defects in the crystal lattice due to improper control of the annealing parameters.

Instead, Matsuo substantially teaches an ion implantation for implanting the indium ions into the polysilicon layer and an annealing step for diffusing implanted indium ions into the polysilicon layer (as admitted by the Examiner). Accordingly, Matsuo fails to teach or disclose at least a step of forming an indium doped polysilicon layer over the gate dielectric layer by using a chemical vapor deposition process using a gas comprising indium chloride ($InCl_3$) as required by the amended proposed independent claim 1, and therefore Matsuo cannot possibly anticipate the amended

proposed independent claim 1 in this regard. Therefore, for at least the foregoing reasons, Applicants respectfully submit that Claim 1 patently defines over Matsuo. Reconsideration and withdrawal of the above rejections is respectfully requested.

Discussion of the claim rejection under 35 USC 103

The Office Action rejected claims 2 and 8-10 under 35 USC 103(a) as being unpatentable over Matsuo in view of Yao et al. (US-6,455,330, hereinafter Yao) and in view of Gerritsen et al. (US-6,281,556, hereinafter Gerritsen).

In rejecting the above claims, the Office Action states that Matsuo discloses every feature of the claimed invention except for in-situ doping method for forming the indium doped polysilicon layer. However, relied upon Yao to disclose the step of forming the indium doped polysilicon layer by performing an in-situ indium ion doping during a chemical vapor deposition operature (col. 8, lines 5-25).

Furthermore, the Office Action states that the combined teachings of Matsuo and Yao teach every feature of the claimed invention as described above except for failing to teach using indium chloride as the dopant source for indium. However, the Office Action relied upon Gerritsen to disclose the use of indium chloride as dopant source for indium (col. 3, lines 5-21).

Applicants respectfully disagree and would like to point out that like Matsuo, both Yao and Gerritsen also substantially teach a step of implanting indium ions. Wherein, at col. 8, lines 11-15, Yao expressly teaches that [polysilicon, after deposition, can be in-situ doped with an p-type impurity such as indium, and Gerritsen, at col. 3,

lines 9-20, teaches a step of implanting indium ions into the substrate. In other words, both Yao and Gerritsen fail to teach, suggest or hint a step of performing the CVD process using a gas comprising indium chloride ($InCl_3$) or a gas mixture comprising indium chloride ($InCl_3$), SiH4, nitrogen and argon to form an indium doped polysilicon layer, as required by the amended claims 1 and 8, respectively.

Claims 2, 9-10 and 21-22 which depend from Claims 1 and 8, directly or indirectly, are also patentable over Matsuo, Yao and Gerritsen, at least because of their dependency from their allowable base claim.

For at least the foregoing reasons, Applicants respectfully submit that claims 1-2, 8-10 and 21-22 patently define over Matsuo, Yao and Gerritsen, and therefore should be allowed. Reconsideration and withdrawal of the above rejections is respectfully requested.

Customer No.: 31561
Application No.: 10/708,175
Docket No.: 11836-US-PA

CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-2, 8-10 and 21-22 of the present application patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted

Date : January 13, 2005

Belinda Lee

Registration No.: 46,863

Jianq Chyun Intellectual Property Office
7th Floor-1, No. 100
Roosevelt Road, Section 2
Taipei, 100
Taiwan
Tel: 011-886-2-2369-2800
Fax: 011-886-2-2369-7233
Email: belinda@jcipgroup.com.tw
Usa@jcipgroup.com.tw